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PRIEST & GOLDSTEIN PLLC
5015 SOUTHPARK DRIVE
SUITE 230
DURHAM, NC 27713-7736

EXAMINER	
RAMPURIA, SATISH	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,855	PITSIANIS ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This action is in response to the amendment filed on 12/14/2004.

2. The objection to claims 11, 15, 18, and 36 is withdrawn in view of applicant's amendment.

1. The rejection under 35 U.S.C. §101 to claims 1, 15, 16, and 18 is still stand rejected.

2. Claims amended by the applicant: 1, 2, 11, 15, 18, 19, 20, 34, and 36.

3. Claims pending in the application: 1-36.

Claim Rejections - 35 USC § 101 Utility

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1, 15, 16, and 18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims are non-statutory because they recite components of allocating memory for VLIW, representing functional descriptive material without a computer readable medium or computer implemented, method per se are not tangibly embodied. Claims 2-14 are directly or indirectly dependent on claim 1, claim 17 is dependent on claim 16, and further support the method of allocating memory for VLIW without a computer readable medium or computer implemented, method per se are not tangibly embodied.

To overcome this type of 101 rejection the claims need to be amended to include the physical computer media or computer implemented method.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 10, 11, 12, 13, 14, 15, 19, and 28-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,930,508 to Faraboschi et al. (hereinafter called Faraboschi) in view of US Patent No. 6,305,014 to Roediger et al. (hereinafter called Roediger).

Per claims 1 and 10:

Faraboschi disclose:

- A method of indirect very long instruction word (VLIW) instruction memory (VIM) allocation (col. 3, lines 1-2 "method for storing and decoding instructions for a microprocessor") comprising the steps of:
- identifying a plurality of VLIW instructions in an input source program (col. 3, lines 2-3 "identifying each word of an instruction");
- allocating at least some of the plurality of VLIW instructions VIM based on the lifetime of each of said plurality of VLIW instructions (col. 3, lines 13-15 "stores instructions in the same format resulting in better utilization of on-chip cache memory").

Faraboschi does not explicitly disclose determining a lifetime of each of said plurality of VLIW instructions.

However, Roediger discloses in an analogous computer system determining a lifetime of each of said plurality of VLIW instructions (col. 1, lines 62-65 "determining the lifetimes of fixed registers in the computer program. By determining the lifetimes of fixed registers, the instruction scheduler can achieve a schedule that has a higher degree of parallelism").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of determining the lifetime of the registers as taught by Roediger into the method of storing and decoding instructions for a microprocessor as taught by Faraboschi. The modification would be obvious because of one of ordinary skill in the art would be motivated to determine lifetime for VLIW instruction to provide faster execution of computer program as suggested by Roediger (col. 1, lines 37-57).

Per claims 11, 12:

The rejection of claim 1 is incorporated, and further, Faraboschi doe not explicitly disclose shortening the life of a particular VLIW by placing an initialization LV statement adjacently prior to the use of its corresponding XV statement.

However, Roediger disclose in an analogous computer system shortening the life of a particular VLIW by placing an initialization load VLIW (LV) statement (col. 10, lines 37-43 "The instructions is removed from the conditional dependence graph... instruction is analyzed to determine if it has a conditional dependence on another instruction... If... instructions... conditional dependence... begin an independent lifetime of a bottleneck...") adjacently prior to the use of its corresponding execute VLIW (XV) statement (col. 10, lines 49-52 "instructions...

lifetime of the bottleneck... defined... instructions... scheduled prior to any instruction in other lifetime").

The feature of shortening the life of a particular VLIW by placing an initialization LV statement adjacently prior to the use of its corresponding XV statement would be obvious for the reasons set forth in the rejection of claim 1.

Per claims 13 and 14:

The rejection of claim 1 is incorporated, and further, Faraboschi doe not explicitly disclose utilizing a coalescing heuristic to reduce VIM requirements of a program.

However, Roediger disclose in an analogous computer system utilizing a coalescing heuristic to reduce VIM requirements of a program (col. 10, lines 59-63 "First we select the sub instruction... remove the sub instruction from the conditional dependence graph". Also, fig. 12 and related discussion).

The feature of utilizing a coalescing heuristic to reduce VIM requirements of a program would be obvious for the reasons set forth in the rejection of claim 1.

Per claim 15:

Faraboschi disclose:

- A method of optimizing the execution time of a user program by reducing redundant loads of very long instruction word (VLIW) instruction memory (VIM) (col. 2, lines 66-67 "The present invention includes an instruction encoding method to reduce or eliminate NOPs in VLIW instructions") comprising the steps of:

- selecting a load ~~VIM~~ VLIW (LV) instruction in a current node (col. 3, lines 2-3 "identifying each word of an instruction that does not contain a NOP code"); and

Faraboschi doe not explicitly disclose placing the LV instruction in a new node which is closer to a program start node.

However, Roediger disclose in an analogous computer system placing the LV instruction in a new node which is closer to a program start node (col. 10, lines 37-43 "The instructions is removed from the conditional dependence graph... instruction is analyzed to determine if it has a conditional dependence on another instruction... If... instructions... conditional dependence... begin an independent lifetime of a bottleneck..."). The limitation regarding the execution frequency in the body of the claim does not given any patentable weight because the preamble of the claim does not recite any limitation related to execution frequency.

The feature of shortening the life of a particular VLIW by placing an initialization LV statement adjacently prior to the use of its corresponding XV statement would be obvious for the reasons set forth in the rejection of claim 1.

Claims 19, 28-31, 32, 33 are the apparatus claim corresponding to method claims 1, 10-14, 11, 15 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1, 10-14, 11, 15 respectively, above.

8. Claims 2, 3, 4, 5, 6, 7, 8, 9, and 20-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi, Roediger in view of US Patent No. 6,675,380 McKinsey et al. (hereinafter called McKinsey).

Per claim 2:

Neither Faraboschi nor Roediger explicitly disclose determining a control flow graph for the input source program containing said plurality of VLIW instructions; determining a VLIW flow graph for said plurality of VLIW instructions; and determining VLIW interference graph.

However, McKinsey discloses in an analogous computer system determining a control flow graph for the input source program containing said plurality of VLIW instructions (col. 5, lines 29-30 "The control flow graph... is made up of blocks of instructions". Also, see fig. 7 and related discussion); determining a VLIW flow graph for said plurality of VLIW instructions (col. 5, lines 31-32 "Each block... contains one or more instructions that will execute in an order defined by the control follow graph". Also, see fig. 7 and related discussion); and determining VLIW interference graph (col. 5, lines 31-32 "Each block... contains one or more instructions that will execute in an order defined by the control follow graph". Also, see fig. 7 and related discussion).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of using control flow graph to determine instructions (VLIW) as taught by McKinsey into the method of storing and decoding instructions for a microprocessor as taught in combination system by Faraboschi and Roediger. The modification would be obvious because of one of ordinary skill in the art would be motivated to

use control flow graph to improve the instruction execution performance of a processor as taught by McKinsey (col. 1, lines 55-67).

Per claim 3:

The rejection of claim 2 is incorporated, and further, Neither Faraboschi nor Roediger explicitly disclose solving VLIW flow equations.

However, McKinsey discloses in an analogous computer system solving VLIW flow equations (figs. 10, 11, 13A and 13B).

The feature of solving VLIW flow equations would be obvious for the reasons set forth in the rejection of claim 2.

Per claims 4, 5:

The rejection of claim 2 is incorporated, and further, Neither Faraboschi nor Roediger explicitly disclose a plurality of nodes which correspond to basic blocks of the VLIW instructions; and a plurality of edges, wherein each edge corresponds to a jump or a call from a given basic block to another basic block.

However, McKinsey discloses in an analogous computer system a plurality of nodes which correspond to basic blocks of the VLIW instructions (col. 4, lines 63-64 "blocks... referred to as nodes in the control flow graph"); and a plurality of edges, wherein each edge corresponds to a jump or a call from a given basic block to another basic block (col. 5, lines 39-

41 "The directed edge determine the relationship between predecessor blocks and successor blocks in the control flow graph").

The feature of plurality of nodes which correspond to basic blocks and edges corresponds to a jump or a call from a given basic block to another basic block would be obvious for the reasons set forth in the rejection of claim 2.

Per claims 6 and 7:

The rejection of claim 5 is incorporated, and further, Neither Faraboschi nor Roediger explicitly disclose determining live-in sets and live-out sets for each of said plurality of nodes and wherein the VLIW flow graph comprises the control flow graph and the live-in sets and live-out sets for each of said plurality of nodes.

However, McKinsey discloses in an analogous computer system determining live-in sets and live-out sets for each of said plurality of nodes (col. 4, lines 63-64 "blocks... referred to as nodes in the control flow graph" and col. 10, lines 6-9 "The method begins... determines... computers a "live on exit" value") and wherein the VLIW flow graph comprises the control flow graph and the live-in sets and live-out sets for each of said plurality of nodes (col. 4, lines 63-64 "blocks... referred to as nodes in the control flow graph").

The feature of determining live-in sets and live-out sets and VLIW flow graph comprises the control flow graph and the live-in sets and live-out sets would be obvious for the reasons set forth in the rejection of claim 5.

Per claim 8:

The rejection of claim 7 is incorporated, and further, Neither Faraboschi nor Roediger explicitly disclose determining an interference graph in which every node of the interference graph corresponds to one of said plurality of VLIW instructions.

However, McKinsey discloses in an analogous computer system determining an interference graph in which every node of the interference graph corresponds to one of said plurality of VLIW instructions (col. 6, lines 42-44 "The dependence graph... includes nodes... each representing a single instructions").

The feature of determining an interference graph for VLIW instructions would be obvious for the reasons set forth in the rejection of claim 7.

Per claim 9:

The rejection of claim 8 is incorporated, and further, Neither Faraboschi nor Roediger explicitly disclose inserting an undirected edge into the interference graph between two VLIW nodes if the two VLIW instructions belong to a live-out set of the same node of the VLIW flow graph; and coloring the interference graph nodes such that adjacent interference nodes are colored in different colors and each color corresponds to a different VIM line.

However, McKinsey discloses in an analogous computer inserting an undirected edge into the interference graph between two VLIW nodes if the two VLIW instructions belong to a live-out set of the same node of the VLIW flow graph (col. 5, lines 39-41 "The directed edges determine the relationship between predecessor blocks and successor blocks in the control follow graph"); and coloring the interference graph nodes such that adjacent interference nodes are

colored in different colors and each color corresponds to a different VIM line. It would be obvious for one skilled in the art to color the graph nodes to distinguish from one another.

The feature of determining an interference graph for VLIW instructions would be obvious for the reasons set forth in the rejection of claim 8.

Claims 20-27 are the apparatus claim corresponding to method claims 2-9 respectively, and rejected under the same rational set forth in connection with the rejection of claims 2-9 respectively, above.

9. Claims 18 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKinsey in view of Faraboschi and further in view of the published document by Chaitin (hereinafter called Chaitin) in 1982.

Per claim 18:

McKinsey disclose:

- determining an interference graph comprising VLIW nodes in which every VLIW node of the interference graph corresponds to one VLIW instruction (col. 6, lines 42-44 "The dependence graph... includes nodes... each representing a single instructions");
- inserting an undirected edge into the interference graph between two VLIW nodes if the two VLIW instructions belong to a live-out set of the same node of the VLIW flow graph (col. 5, lines 39-41 "The directed edges determine the relationship between predecessor blocks and successor blocks in the control follow graph"); and

Mckinsey does not explicitly discloses VLIW instruction.

However, Faraboschi discloses in an analogous computer a method for compacting VLIW instructions.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of compacting the VLIW instructions as taught by Faraboschi into the method of storing and decoding instructions for a microprocessor as taught by McKinsey. The modification would be obvious because of one of ordinary skill in the art would be motivated to use control flow graph to improve the instruction execution performance of a processor as taught by McKinsey (col. 1, lines 55-67).

Neither McKinsey nor Faraboschi discloses coloring the VLIW graph nodes such that adjacent VLIW nodes are colored in different colors and each color corresponds to a different VIM line.

However, Chaitin discloses in an analogous computer coloring the VLIW graph nodes such that adjacent VLIW nodes are colored in different colors and each color corresponds to a different VIM line (page 99, section 2. OVERVIEW OF REGISTER ALLOCATION "...Next we use the... observation in order to construct a 32-coloring... find a 32-coloring of graph G havin a not N of degree less that 32...reduced graph G' only has nodes of degree 32 or greater").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of coloring the graph differently as taught by Chaitin into the method of storing and decoding instructions for a microprocessor as taught by the combination system of McKinsey and Faraboschi. The modification would be obvious

because of one of ordinary skill in the art would be motivated to use the coloring technique to improve the performance of CPU as taught by Chaitin (page 98, section 1.Introduction).

Claim 36 is the apparatus claim corresponding to method claim 18 and rejected under the same rational set forth in connection with the rejection of claim 18 above.

10. Claims 16-17 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKinsey in view of Faraboschi.

Per claims 16-17:

McKinsey disclose:

- A method to statically determine liveness of indirect very long instruction word (VLIW) instructions (col. 10, lines 7-9 "determines whether I is a store or a branch instructions, or if I computes a "live on exit" value") comprising the steps of:
- determining a control flow graph which includes nodes representing basic program blocks (col. 4, lines 63-64 "blocks... referred to as nodes in the control flow graph"), and edges connecting the nodes which represent jumps and calls from one block to another block (col. 5, lines 39-41 "The directed edge determine the relationship between predecessor blocks and successor blocks in the control flow graph"); and
- determining a VLIW flow graph by solving VLIW flow equations (figs. 10, 11, 13A and 13B).

Mckinsey does not explicitly discloses VLIW instruction.

However, Faraboschi discloses in an analogous computer a method for compacting VLIW instructions.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of compacting the VLIW instructions as taught by Faraboschi into the method of storing and decoding instructions for a microprocessor as taught by McKinsey. The modification would be obvious because of one of ordinary skill in the art would be motivated to use control flow graph to improve the instruction execution performance of a processor as taught by McKinsey (col. 1, lines 55-67).

Claims 34-35 are the apparatus claim corresponding to method claims 16-17 respectively, and rejected under the same rational set forth in connection with the rejection of claims 16-17 respectively, above.

Response to Arguments

11. Applicant's arguments with respect to claims have been considered but they are not persuasive.

In the remarks, the applicant has argued that:

(i) Applicants do not acquiesce with the Examiner's analysis of 35 U.S.C. § 101 rejection to claims 1-18, Applicants believe that claim are directed to method which is clearly patentable subject matter.

(ii) Faraboschi addresses a totally different problem of compacting VLIW instructions by eliminating NOP codes form an instructions as compare to present invention

addresses techniques for allocating VLIW instructions to VLIW instructions memory (VIM) as claimed in claim 1.

(iii) Roediger does not address "allocating at least some of the plurality of VLIW instructions to VIM base on the lifetime of said plurality of VLIW instructions" as claimed in claim 1.

Examiner's response:

(i) Regarding the analysis on rejection given by the Examiner is proper (see MPEP chapter 700). Claims are directed to method only the steps in claims could be performed by one skilled in the art on the pencil and paper, no computer needed. To fix this issue please amend the claims to computer implemented method.

(ii) Regarding the limitation allocating VLIW instructions to VLIW instructions memory (VIM), Faraboschi discloses compacting or optimizing the VILW instructions for storing compact instructions where Faraboschi eliminates the NOP instructions to save the storage area which is similar to efficiently allocating VILW instructions to memory as disclosed in present invention (see Applicant's specification, page 2, lines 5-15). Therefore, the rejection is proper and maintained herein.

(iii) Regarding Roediger does not address "allocating at least some of the plurality of VLIW instructions to VIM base on the lifetime of said plurality of VLIW instructions" as claimed in claim 1. It should be noted by the Applicants that Roediger used to reject the limitation "determining a lifetime of each of said plurality of VLIW instructions" (see the rejection above and previous office action). Applicant

only makes general allegations and does not point out any errors in the rejection. Rather, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, the rejection is proper and maintained herein.

12. Applicant's arguments with respect to claims 16-18 and 34-36 has been considered but are moot in view of new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571)** 272-3732. The examiner can normally be reached on **8:30 am to 5:00 pm**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Tuan Q.** Dam can be reached on **(571) 272-3695**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner
Art Unit 2124
05/31/2005

WEI Y. ZHEN
PRIMARY EXAMINER